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Filed : December 3, 1999

The Examiner also objected to the drawings as failing to comply with 37 C.F.R. §1.84(p)(4) because “the reference characters ‘28a’ and ‘22’ in Fig. 1B have both been used to designate the electrode.” Applicants respectfully submit that as indicated in the specification on page 4, reference character ‘22’, now reference character ‘22a,’ refers to the electrode while reference character ‘28a’ refers to the HSG silicon microstructure. Reference character ‘28a’ thus indicates a specific feature of the electrode ‘22a.’ This is indicated in the figure by the line from reference character ‘28a’ to the specific feature of the electrode. As the reference characters refer to different structures, Applicants submit that no correction is required.

Claim rejections under 35 U.S.C. §103(a)

All claims stand rejected under 35 U.S.C. §103(a) as being unpatentable over a combination of references. In particular, each rejection is based on the teachings of U.S. Patent No. 4,058,430 to Suntola et al. (the ‘430 patent) and U.S. Patent No. 5,650,351 to Wu (the ‘351 patent). The Examiner argues that “it would have been obvious to one having ordinary skill in the art to combine the teachings of Suntola et al. with the invention disclosed by Wu since Wu discloses a highly dielectric layer and Suntola et al. teach a process to form a dielectric layer that will have a high dielectric constant.”

In order to establish a prima facie case of obviousness, the Examiner must show that there was some suggestion or motivation to combine reference teachings. Further, the Examiner must show that there was a reasonable expectation of success. M.P.E.P. §706.02(j). Applicants submit that here the Examiner has provided no evidence of motivation to combine reference teachings and has failed to demonstrate that there was a reasonable expectation of success. As a result, the Examiner has not met his burden of establishing a prima facie case of obviousness and this rejection should be withdrawn.

“To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the invention to have been obvious in light of the teachings of the references.” *Ex parte Clapp* 227 U.S.P.Q. 972, 973 (Bd Pat. App. & Inter. 1985). There is no suggestion in the cited references to use ALD processes to deposit dielectric layers on HSG. Wu teaches a method of forming a

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capacitor in which a dielectric layer is deposited on HSG but does not suggest or indicate that using ALD would be beneficial. The Suntola et al. reference fails to disclose or suggest using ALD to deposit on HSG silicon.

The lack of suggestion in the references themselves is not made up for by the Examiner's arguments. In fact, the Examiner has provided no evidence as to why the skilled artisan would have been motivated to combine the two references. HSG and ALD have both been independently known for approximately twenty years. Yet in all that time, no reference has been produced showing the combination of ALD and HSG. The Examiner has failed to provide a reference that even suggests a combination of the two. Further, a need in the art that would be met by a combination of the two references has not been described. Applicants submit that as the Examiner has failed to provide a convincing line of reasoning as to why the skilled artisan would be motivated to combine the cited references, a prima facie case of obviousness has not been made.

Further, the Examiner has not shown any reasonable expectation of success in combining the references. The combination of HSG and high-k dielectrics, regardless of how they are formed, has been treated as incompatible in the literature. Most known high-k deposition processes require the use of highly oxidizing environments and high temperatures during the deposition process and later during an anneal step. Under these conditions the underlying polysilicon would be oxidized. This would create a layer of silicon oxide with a low dielectric constant, thus decreasing capacitance. In addition, the benefit of the increased surface area obtained by the use of HSG silicon would be reduced by oxidation.

As stated in U.S. Patent No. 6,107,136 to Melnick et al., a copy of which is enclosed, "high-k materials may be incompatible with many commonly used electrode materials because they require high temperature anneals in oxygen or deposition at high temperatures in the presence of oxygen in order to achieve their desired electrical properties. The exposure to oxygen at high temperatures is problematic because it can result in an oxidation of the electrode. This, in turn, can produce changes in the electrical properties of the capacitor." (column 1, lines 24-28). As high-k processes are not readily integrated with silicon bottom electrodes, the art has focused on using metal bottom electrodes in combination with high-k dielectrics. "In order to minimize the problems associated with oxidation, materials that are resistant to oxidation at high

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temperatures and materials which form conductive oxides, such as platinum, iridium, palladium, ruthenium, osmium, and the like are being investigated for use in forming electrodes." *Id.* at column 1, lines 32-37. Thus, one of ordinary skill in the art would not have had a reasonable expectation of success in combining an HSG bottom electrode with ALD of a high-k dielectric.

The Examiner has provided no evidence of a suggestion or motivation to combine references and the skilled artisan would not have had a reasonable expectation of success in combining the references. Thus, a prima facie case of obviousness has not been made. As all of the rejections are ultimately based on this combination of references, Applicants respectfully request that the rejections be withdrawn.

CONCLUSION

For the reasons presented above, Applicants submit that all pending claims are in condition for allowance and an early action to that effect is respectfully solicited. If any issues remain or require further clarification, the Examiner is requested to call Applicants' counsel at the number listed below in order to resolve such issues promptly.

Respectfully submitted,

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